

Scheduling for Time-Triggered Network Communication

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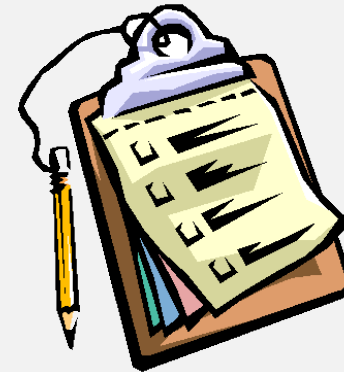


(1) Rückblick

(2) Verwandte Arbeiten

- Heuristiken
- Model Checking (SPIN)
- Model Checking (UPPAAL)

(3) Ausblick



- Time-Triggered Ethernet (TTTech)
- Echtzeiterweiterung
- Switched bussystem

- Schedulingproblem: NP-vollständig
- Preemptive und non-preemptive
- Statisch und dynamisch

- **Time Triggered**

- Zeitkritischer Netzwerkverkehr
- Höchste Priorität
- Minimum an Latenz und Jitter

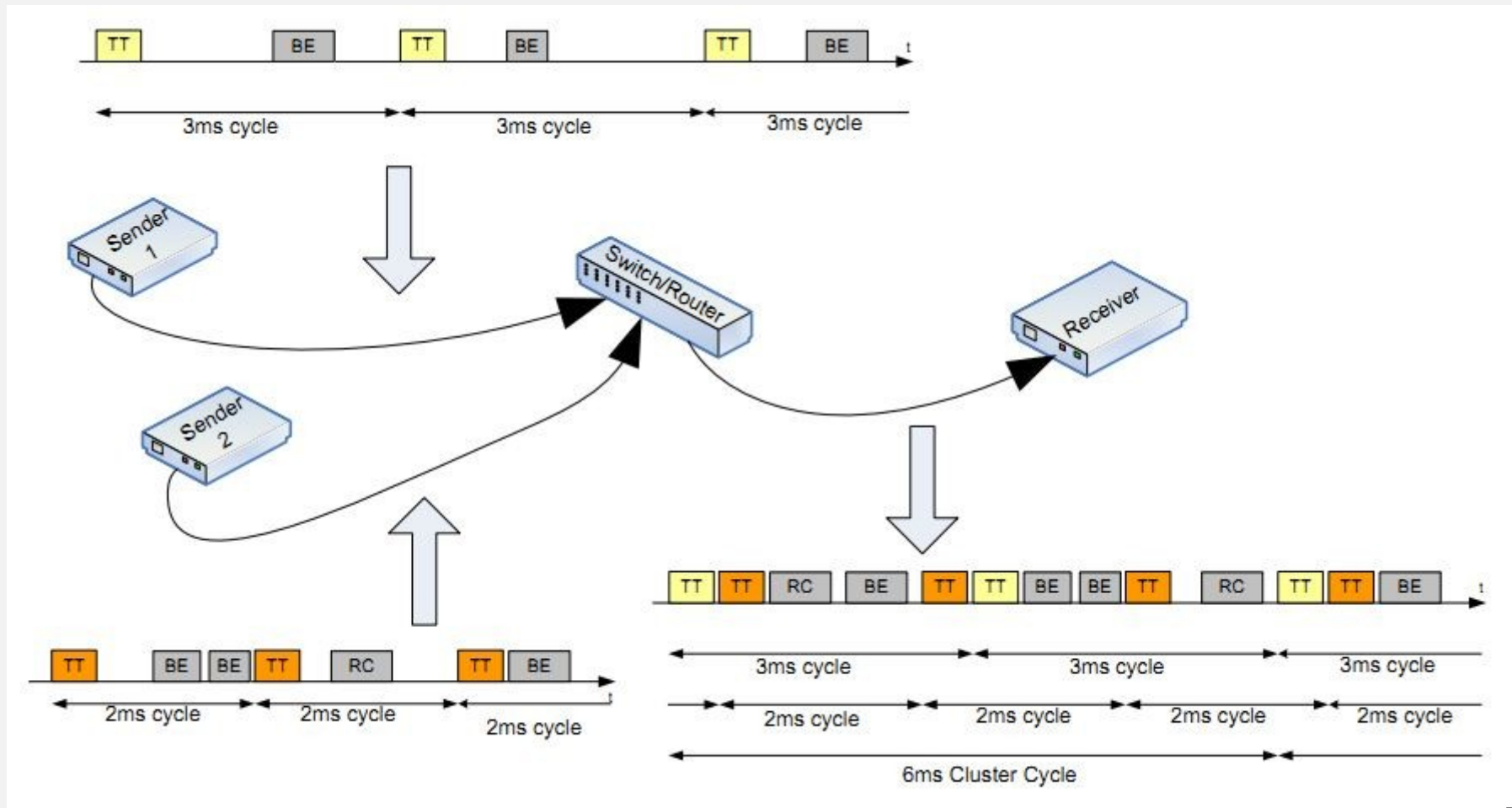
- **Rate-constrained**

- Ereignisbasierter Nachrichtentyp
- Unterliegt keinem festen Scheduling
- Werden von TT-Nachrichten verdrängt

- **Best-efford**

- Standard Ethernet Netzwerkverkehr

Rückblick: TTE-Schedule



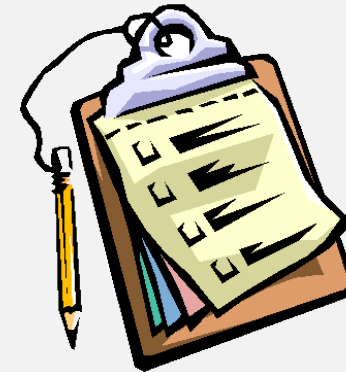
[1]

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Scheduling with Bus Access Optimization for Distributed Embedded Systems

- Mehrere programmierbare und Hardware Prozessoren
- TTP Bussystem
- Netzwerk-Tasks als normale Prozess-Tasks
- Kontroll- und Datenabhängigkeiten



Alex Doboli
Linköping University



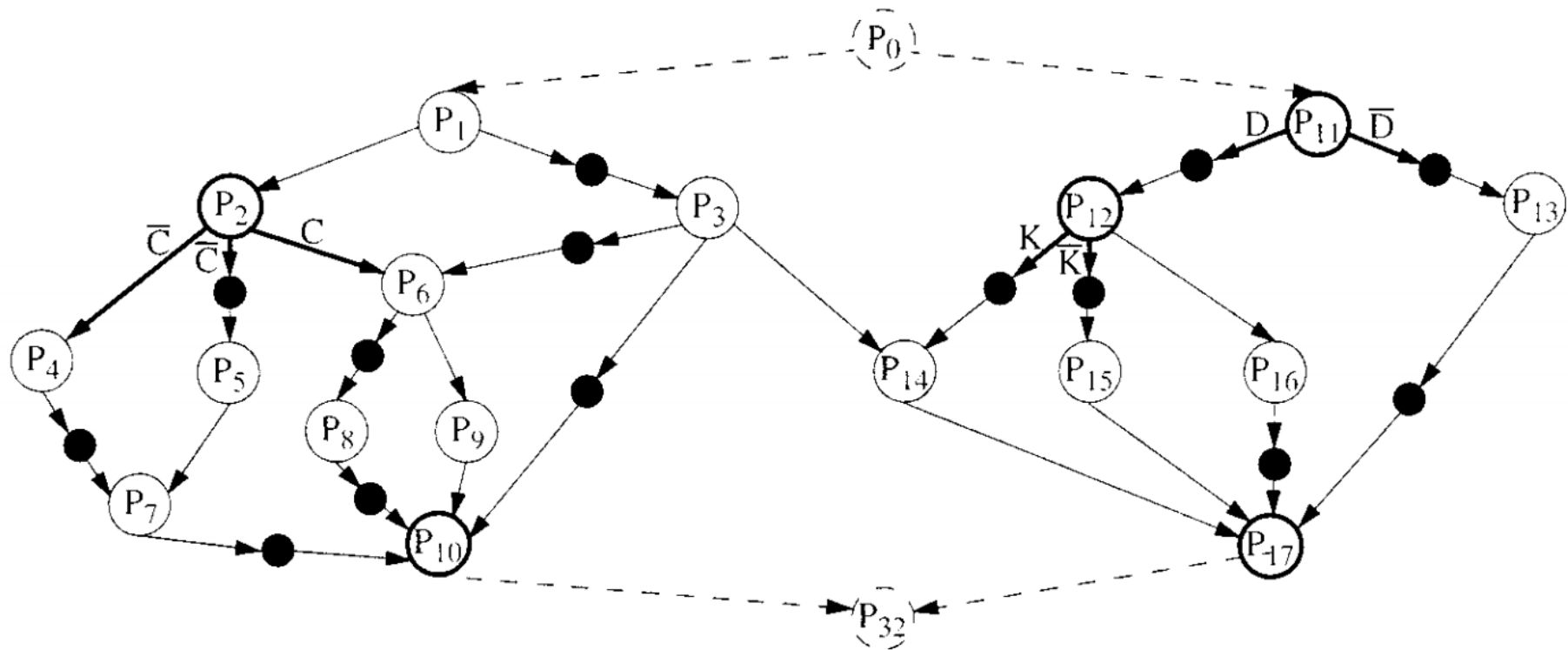
Paul Pop
Linköping University



Petru Eles
Linköping University



Zebo Peng
University of Cincinnati



Conditional Process Graph

$$G = (V, E_s, E_c)$$

[2]

```
List_schedule ()  
  for each processing element  $pe_i, i=1,2, \dots, N_{pe}$ , do  
     $free_{pei}=0$   
  end for;  
  schedule  $P_0$  at  $t=0$ ; initialize ready process list  $Ls\_Ready$   
  with direct successors of  $P_0$ ;      --  $P_0$  is the source node  
  while  $Ls\_Ready$  is not empty do  
     $p=Head(Ls\_Ready)$ ;  
    if  $M(p) \in HP$  then      -- hardware supports several  
      schedule  $p$  at  $t=p.t_{ready}$  -- processes at a time;  
    else  
       $p=Select(Ls\_Ready, M(p))$ ;  
      schedule  $p$  at  $t=\max(p.t_{ready}, free_{M(p)})$ ;  
       $free_{M(p)}=t+t_p$   
    end if;  
    delete  $p$  from  $Ls\_Ready$ ;  
     $Ls\_Ready = Ls\_Ready +$  processes which become  
      ready after  $p$  is executed  
  end while  
end List_schedule;
```

[2]

Basic list scheduling algorithm

Heuristiken: Schedule Table

	$true$	D	$D \wedge C$	$D \wedge C \wedge \bar{K}$	$D \wedge C \wedge K$	$D \wedge \bar{C}$	$D \wedge \bar{C} \wedge \bar{K}$	$D \wedge \bar{C} \wedge K$	$\bar{D}$	$\bar{D} \wedge C$	$\bar{D} \wedge \bar{C}$
P_1	0										
P_2	3										
P_3		6							6		
P_4						7					7
P_5							18	18			18
P_6				21	20					20	
P_7							21	21			21
P_8				29	28					28	
P_9				26	25					25	
P_{10}				35	34		27	26		34	26
P_{11}	0										
P_{12}			9			9					
P_{13}										10	13
P_{14}					18			24			
P_{15}				19			24				
P_{16}				15	15		15	15			
P_{17}				25	24		30	26		24	24
$P_{18} (1 \rightarrow 3)$	3										
$P_{19} (2 \rightarrow 5)$						9					8
$P_{20} (3 \rightarrow 10)$				21	20		21	20		20	20
$P_{21} (3 \rightarrow 6)$				19	18					18	
$P_{22} (4 \rightarrow 7)$						12					13
$P_{23} (6 \rightarrow 8)$				26	25					25	
$P_{24} (7 \rightarrow 10)$							25	24			24
$P_{25} (8 \rightarrow 10)$				33	32					32	
$P_{26} (11 \rightarrow 13)$										8	11
$P_{27} (11 \rightarrow 12)$			8			8					
$P_{28} (12 \rightarrow 14)$					16			16			
$P_{29} (12 \rightarrow 15)$				16			16				
$P_{30} (13 \rightarrow 17)$										22	22
$P_{31} (16 \rightarrow 17)$				23	22		23	22			
D	6										
C		7							7		
K			15			15					

[2]

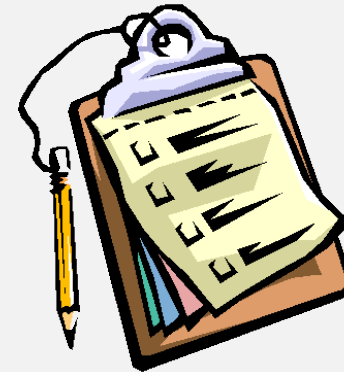
- TTP ist kein TTE
- Keine Betrachtung von Nachrichtenklassen
- Kein reines statisches Scheduling
- Starker Fokus auf Conditions

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Optimization of Static Task and Bus Access Schedules for Time-Triggered Distributed Embedded Systems with Model-Checking

- Programmierbare Prozessoren
- TTP Bussystem
- Software Tasks und Network Messages in statischer Lookup Table
- Process Graph $G = (V, E)$



Zonghua Gu



Xiuqiang He



Mingxuan Yuan

Hong Kong University

- Gerard J. Holzmann – Bell Labs
- Tool zum verifizieren von verteilten Software Modellen
- Promela (Process Meta Language)
- Linear Temporal Logic (LTL)
- Generiert Problem spezifische Model-Checker

```
proctype Task(byte i) {
  {Block until precedence relations are satisfied.}
  /*Block until CPU is free.*/
  atomic{CPU[Task[i].cpuID].status==FREE->
    Task[i].status=RUNNING;
    Task[i].finTime=time+Task[i].et;
    CPU[Task[i].cpuID].status=BUSY;}
  /*Block until time advances to its finish time*/
  atomic{time==Task[i].finTime->
    Task[i].status=DONE;
    CPU[Task[i].cpuID].status=FREE;
    {Send messages to remote receiver tasks.}}
```

[4]

Model of a non-preemptive Task

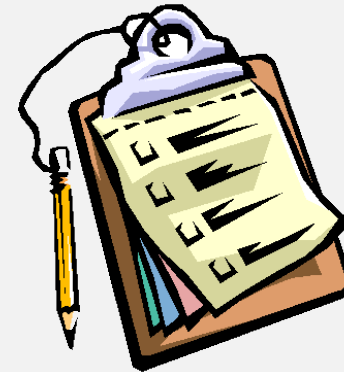
- TTP ist kein TTE
- Liefert bessere Ergebnisse als die vorherige Heuristik
- Betrachtet work- und non work-conserving Scheduling
- Ressourcenintensiv
- State space explosion

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- **Model Checking (UPPAAL)**

(3) Ausblick



Optimal Static Task Scheduling on Reconfigurable Hardware Devices using Model-Checking

- Re-konfigurierbare FPGAs
- Kein verteiltes System
- Schedulingproblem ähnlich
- Parallelität
- UPPAAL



Zonghua Gu



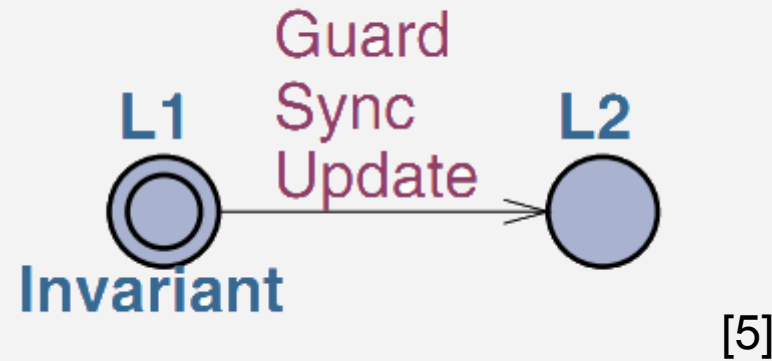
Xiuqiang He



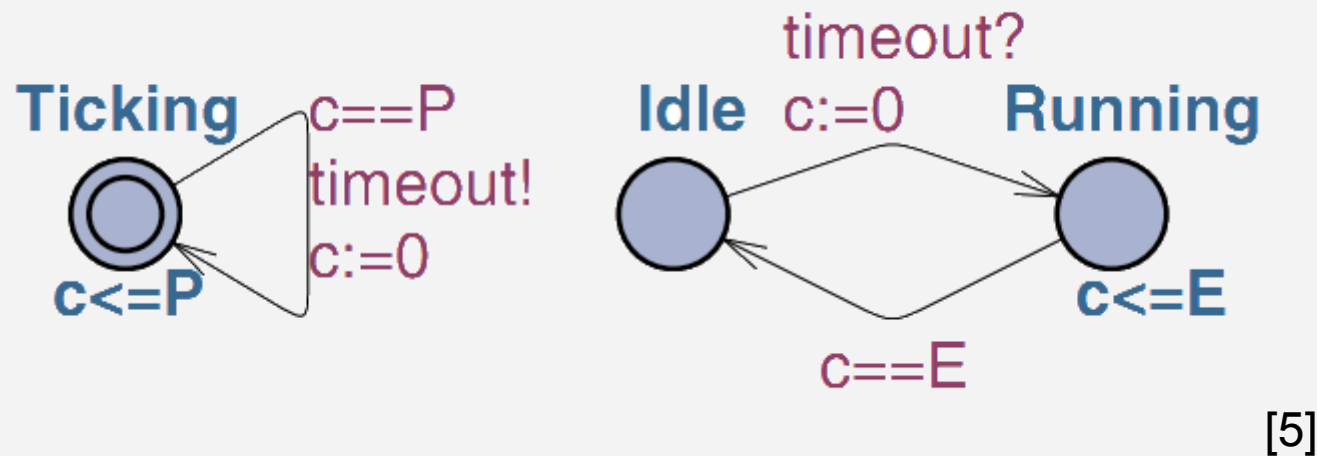
Mingxuan Yuan

Hong Kong University

- Entwickelt von der Uppsala und Aalborg Universität
- Timed Automata
- Synchronisationskanäle
- Integer Variablen
- Timed Computational Tree Logic (TCTL)
- Execution Trace to final reachable state

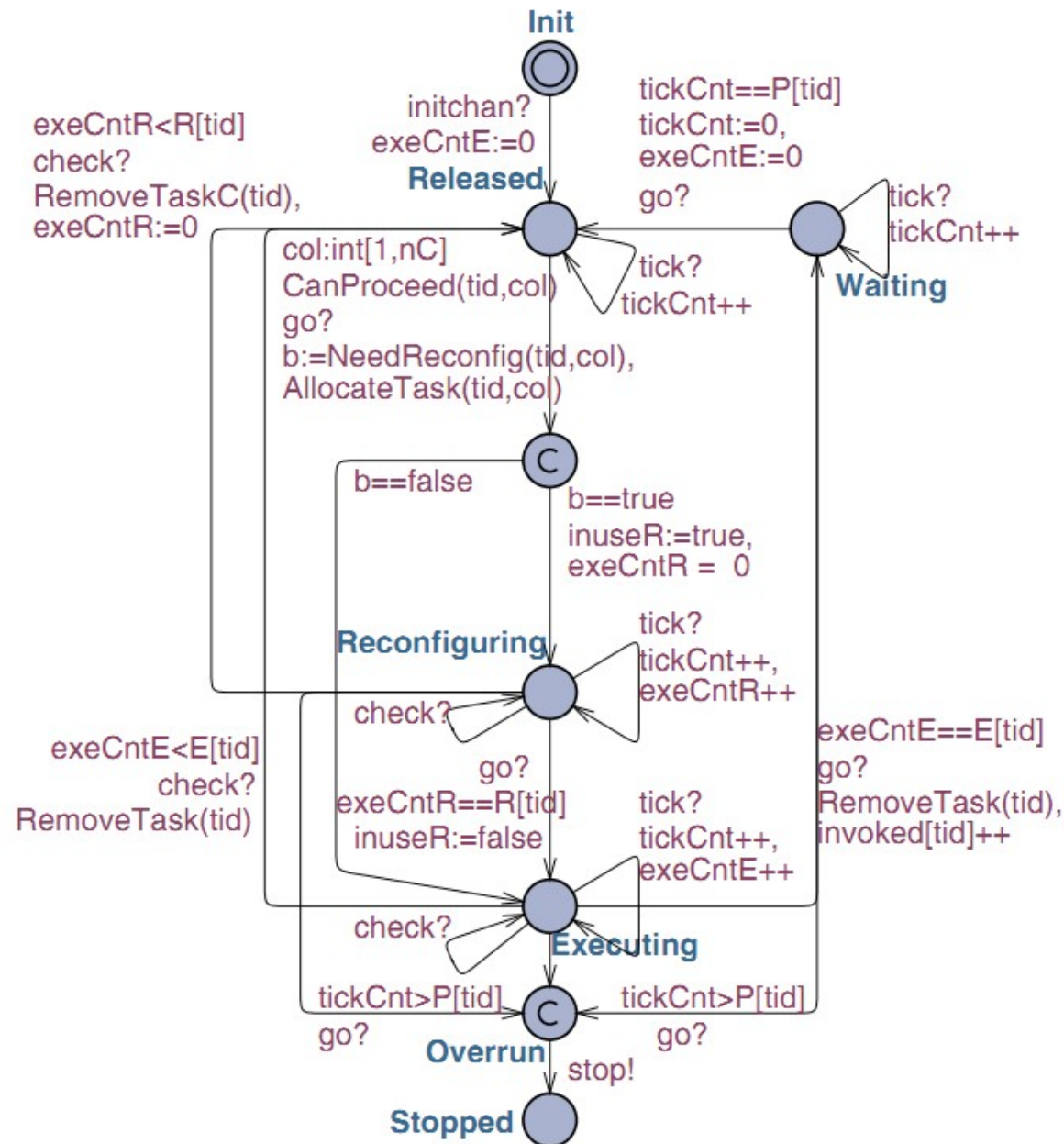


Basis Syntax



Periodic Task System

Model-Checking: UPPAAL



[5]

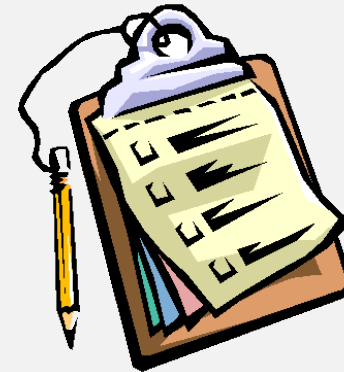
- Timed Automata alternativer Ansatz
- Static Scheduling of real-time tasks
- Parallelität
- Kein verteiltes System
- Kommunikationsprotokoll?
- Nachrichtenklassen?

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- Basis-Tool entwickeln für TTE-Scheduling
- Heuristik oder Model-Checking?
- Wie lassen sich die TTE-Eigenschaften und Nachrichtenklassen integrieren?
- Bisherige Arbeiten beachten nur TTP

Vielen Dank...



für die
Aufmerksamkeit!



Hochschule für Angewandte Wissenschaften Hamburg

Hamburg University of Applied Sciences

- (1) Florian Bartols, Leistungsmessung von Time-Triggered Ethernet Komponenten unter harten Echtzeitbedingungen mithilfe modifizierter Linux-Treiber, 2010
- (2) Petru Eles, Alex Doboli, Paul Pop and Zebo Peng, Scheduling with Bus Access Optimization for Distributed Embedded Systems, 2000
- (3) Paul Pop, Petru Eles, Zebo Peng and Traian Pop, Scheduling and Mapping in an Incremental Design Methodology for Distributed Real-Time Embedded Systems, 2004
- (4) Zonghua Gu, Xiuqiang He and Mingxuan Yuan, Optimization of Static Task and Bus Access Schedules for Time-Triggered Distributed Embedded Systems with Model-Checking, 2007
- (5) Gerard J. Holzmann, The Model Checker SPIN, 1997
- (6) Zonghua Gu, Mingxuan Yuan and Xiuqiang He, Optimal Static Task Scheduling on Reconfigurable Hardware Devices using Model-Checking, 2007
- (7) Fei Yu, Guoqiang Li and Naixue Xiong, Schedulability Analysis of Multi-Processor Real-Time Systems Using Uppaal, 2010

